In the Claims:

1-7. (Cancelled)

8. (Currently Amended) A method of transforming an Orthogonal Frequency Division Multiplexing (OFDM) signal by a fast Fourier transform (FFT) processor, the OFDM signal having a symbol, the symbol including a ~~first long~~ preamble~~, a second long preamble~~ and first data following the preamble, the ~~first and second long preambles respectively~~ preamble having a sequence of N-samples and the first data having a sequence of N/2 samples, the method comprising:

~~(a)~~ storing the ~~first long~~ preamble ~~and the second long preamble in first, second, third and fourth memories in sequence~~ in a memory as the OFDM signal is received;

~~(b)~~ reading the ~~first long~~ preamble from the memory ~~and the second long preamble stored in the first, second, third and fourth memories~~ in response to an end point of the ~~second long~~ preamble being detected, transforming the ~~first and second long preambles~~ preamble by a fast Fourier transform~~, respectively,~~ into a ~~third~~ transformed preamble ~~and a fourth preamble~~, and storing the transformed preamble ~~in sequence the third and fourth long preambles~~ in the ~~first~~ memory ~~and the second memory~~;

buffering first data that follows the preamble while the preamble is transformed;

~~(c)~~ simultaneously transforming second data that is received by the FFT processor after the first data is buffered and that has a sequence of N/2 samples, and the buffered first data, respectively, using an N-point FFT transform into third data as the second data is received ~~when the first and second long preambles are transformed into the third and fourth preambles~~, and

storing the third data in the memory ~~memories in sequence~~, and outputting the third data~~, stored in the memories; and~~

~~(d) finishing the fast Fourier transform method when the symbol is a final symbol, and performing (c) when the symbol is not the final symbol;~~

~~wherein (c) comprises:~~

~~(c-1) activating a first toggle signal that is configured to control read and write operations with respect to the memories when the first long preamble and the second long preamble are transformed by the fast Fourier transform;~~

~~(c-2) determining whether or not the first data are transformed by the fast Fourier transform when the first toggle signal is in an active state;~~

~~(c-3) storing in sequence the third data in the first memory and the third memory when the first and second data are transformed by the fast Fourier transform, and outputting in sequence the third data stored in the second and fourth memories; and~~

~~(c-4) inverting the first toggle signal, and activating a second toggle signal for controlling the read and write operations with respect to the memories.~~

9-11. (Cancelled)

12. (Original) The method according to Claim 8, wherein the first data is delayed data by N/2.

13-20. (Cancelled)

21. (New) The method according to Claim 8, wherein the memory comprises first, second, third and fourth memories each of which is configured to store N/2 samples, wherein transforming the first data and the second data comprises:

activating a first toggle signal that is configured to control read and write operations with respect to the memory when the preamble is transformed by the fast Fourier transform;

determining whether or not the first data are transformed by the fast Fourier transform when the first toggle signal is in an active state;

storing in sequence the third data in the first memory and the third memory when the first and second data are transformed by the fast Fourier transform, and outputting in sequence data stored in the second and fourth memories while the third data are stored in the first and third memories; and

inverting the first toggle signal, and activating a second toggle signal for controlling the read and write operations with respect to the memories.

22. (New) The method according to Claim 21, wherein the first toggle signal controls the read operation with respect to the first and third memories and controls the write operation with respect to the second and fourth memories, and the second toggle signal controls the write operation with respect to the first and third memories and controls the read operation with respect to the second and fourth memory.

23. (New) The method of Claim 8, wherein transforming the first data and the second data into third data comprises supplying the first data from an input buffer to a first input of an FFT processing element and supplying the second data directly from an analog to digital converter to a second input of an FFT processing element without buffering the second data.

24. (New) The method of Claim 23, wherein the first data and the second data are provided to the FFT processing element in response to completion of the step of transforming the first long preamble and the second long preamble.

25. (New) The method of Claim 8, wherein the preamble comprises a first preamble and a second preamble, the method further comprising forming an average of the first preamble and the second preamble, wherein transforming the preamble comprises transforming the average of the first preamble and the second preamble.

26. (New) The method of Claim 8, wherein the memory comprises first, second, third and fourth memories each of which is configured to store N/2 samples, wherein storing the third data comprises storing the third data in the first and third memories, the method further comprising:

transforming fourth and fifth data having respective sequences of N/2 samples into sixth data;

storing the sixth data in the second and fourth memories; and

outputting the third data from the first and third memories while the sixth data is stored.

27. (New) The method of Claim 8, further comprising finishing the fast Fourier transform method when the symbol is a final symbol, and repeating buffering first data and transforming first and second data when the symbol is not the final symbol.

28. (New) A Fast Fourier Transform (FFT) processor for demodulating an orthogonal frequency division multiplexing (OFDM) signal including a preamble having a sequence of N samples and first data following the preamble and having a sequence of N/2 samples, the FFT processor comprising:

a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the preamble;

a controller that is configured to output a first control signal and a second control signal in response to the timing signal;

a signal converter that is configured to store the preamble in response to the first control signal, to transform the preamble by an N-point FFT into a second preamble, and to store the second preamble; and

an FFT input buffer that is configured to store the N/2 samples of the first data while the preamble is being transformed, wherein the signal converter is further configured to perform an N-point FFT of the buffered first data and second data having a sequence of N/2 samples as the second data is sequentially received to transform the first data and the second data into third data having N samples.

29. (New) The FFT processor of Claim 28, further comprising:

a frequency domain equalizer that is configured to synchronize the second preamble and the third data in response to the second control signal with a clock frequency of the fast Fourier transform processor, and to output the synchronized second preamble and the third data.

30. (New) The FFT processor of Claim 28, further comprising an analog to digital converter (ADC), wherein the FFT buffer is coupled to the ADC and receives the first data from the ADC and wherein the signal converter is coupled to the ADC and receives the first

data as buffered data from the FFT input buffer and receives the second data as unbuffered data from the ADC.

31. (New) The FFT processor of Claim 30, wherein the FFT input buffer is configured to delay the first data by N/2 samples.

32. (New) The FFT processor of Claim 30, wherein the signal converter comprises an FFT processing element including a first input line configured to receive a sample of the first data and a second input line configured to receive a sample of the second data.

33. (New) The FFT processor of Claim 30, further comprising:

a quadrature detector that is configured to receive the OFDM signal, to convert the OFDM signal into a baseband OFDM signal, to generate a real component of the OFDM signal and an imaginary component of the OFDM signal, and to output the real component of the OFDM signal and the imaginary component of the OFDM signal to the ADC.